REMARKS

Claims 22-39 are pending in the application. In response to the Office Action, applicants have amended the drawings and the specification, and amended claims 22, 28, and 34. Claims 22-39 remain pending for reconsideration.

The drawings were objected to under 37 C.F.R. § 1.83(a) because of aspects of the newly presented claims not being illustrated in the drawings. Applicants have amended the drawings in accordance with the Examiner's suggestion. Support for the drawing change may be found in the textual description for example, at least at page 9, lines 11-20. The specification has been amended editorially in accordance with the requested drawing change. No new matter has been added.

Claims 22-39 were rejected under 35 U.S.C. § 112, first paragraph. Applicants respectfully traverse this rejection for the following reasons.

Applicants first note that the Examiner's position with respect to the 112, first paragraph rejection is inconsistent with the Examiner's position with respect to the § 103 rejection. In most of the different 112 rejections, the Examiner asserts that the supposed unsupported or non-enabled claim language would be unclear to one skilled in the art as to how to make or use the invention without undue experiment. However, the Examiner then asserts in the § 103 rejection that each element is found in the prior art and would be obvious to one skilled in the prior art. If the rejections are maintained, the Examiner should cure this inconsistency.

With respect to claims 22, 28, and 34, the Examiner objects to the claim language relating to identifying a race condition in a circuit. Applicants disagree with the Examiner's position, but have deleted this language from these claims, rendering this rejection moot. Applicants note that the deletion of the respective phrases is a broadening amendment, and applicants do not surrender any claim scope or equivalents by way of the present amendments.

With respect to claims 25, 31, and 37, the rejection is not understood. The Examiner objects to the phrase "with a physical characteristic of the circuit" even though the Examiner has identified corresponding support in the specification that explicitly states "characteristics of the physical circuit" at page 8, lines 10-12. Applicants submit

that this portion alone provides ample support for the claim language. Literal word for word support for the claim language is not required so long as one skilled in the art would appreciate that the claim language is supported by the description and the drawings. In any event, reference is made throughout the specification to various physical characteristics of the circuit including the non-limiting examples of "exact delay characteristics" (page 8, lines 10-12), "die and chip architecture constraints" (page 2, line 8), operational speed of gates (page 2, line 9), "the lengths of conductive paths between circuit elements" (page 2, lines 9-10), and "specific routing directions and positions of each element" (page 2, line 10). Those skilled in the art would appreciate that other physical characteristics of the circuit may also be covered by the claim language. Accordingly, applicants submit that the claim language is supported in the original disclosure and that one skilled in the art would understand how to specify the virtual clock signal in accordance with a physical characteristic of the circuit, and the rejection should be withdrawn.

With respect to claims 27, 33, and 39, the Examiner is unable to find support for the claim language relating to the "length of conductive paths." Support is explicitly provided on page 2, lines 9-10, which describes how a delay in a circuit may be caused by "the lengths of conductive paths between circuit elements." Support is also found in the paragraph on page 2, lines 11-20, which describes how a delay may be caused "if second conductive path 12 is of much greater length than first conductive path 8" (see page 2, lines 11-12). Finally, support is provided by page 6, line 28 through page 7, line 8, which describes how data traveling on like numbered second conductive path 12 takes a long time relative to data traveling on like numbered first conductive path 8. Applicants submit that the present disclosure fully supports the claims and enables one of ordinary skill in the art to understand how the delay characteristic may correspond to a length of conductive paths between circuit elements, and the rejection should be withdrawn.

With respect to claims 23, 29, and 35, the Examiner asserts that the claim language "selectively providing a virtual delay element for respective sequential elements in the circuit" is not enabled. Applicants again note that this position is inconsistent with the Examiner's position in the § 103 rejection that the claim language is taught by the

prior art. In any event, the language is fully supported and enabled. At page 8, lines 14-19, the present specification describes:

> According to an embodiment of the present invention, race resolution at every sequential element can be individually controlled by the introduction of virtual delay elements controlled by corresponding virtual clocks in the appropriate path. Therefore, each sequential element can have its own race resolution mechanism. For example in sequential circuit 29, if control over the arrival time of data1 is required by ATPG, then a virtual delay element 38 may be added along the path of the data1 input to flip-flop 30.

For example, the foregoing describes that race resolution may be determined on an individual basis for each sequential element. For example, the virtual delay element 38 may be provided if the ATPG requires control over the arrival time of data1. For example, in various of the figures, some sequential elements have associated virtual delay elements while others do not. In fact, throughout the specification and drawings, the concept of adding virtual delay elements where such control is needed is described. Applicants submit that the present disclosure more than adequately enables one of ordinary skill in the art to practice claims 23, 29, and 35, and the rejection should be withdrawn.

Claims 22-39 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Zeiner (U.S. Patent No. 5,798,645), in view of Selvidge (U.S. Patent No. 5,649,176) and further in view of Dargelas (U.S. Patent No. 5,938,753). Applicants respectfully traverse this rejection for the following reasons.

By way of background, the invention as presently claimed is directed to the problem of test pattern generation for a circuit which may have a race condition which requires race resolution in order to generate a valid test pattern. None of the cited references are directed to this problem. In fact, Dargelas fails to even mention race resolution, Selvidge mentions race conditions only tangentially in terms of hold time

violations, and Zeiner addresses the problems of race conditions in a physical device with physical delay element.

Applicants first note that is highly unlikely that one of ordinary skill in the art would be motivated to find and make the myriad of modifications required by the combination of the three cited references, absent the benefit of the present specification. With the present amendment of claim 22, the Examiner's primary reference is relied upon for only a single aspect of the claim, namely generating a netlist model. The Examiner admits that the primary reference fails to teach or suggest the recited providing a virtual delay element, providing a virtual clock, and generating a test pattern, and relies on the two other references to piece together the rejection.

Moreover, any motivation to combine the references fails for at least the following reasons. Zeiner has already solved the problem of internal race conditions by the utilization of physical, programmable delay devices. The Examiner has not provided any explanation as to why anyone would be motivated to replace the physical, programmable delay devices in Zeiner with the virtual, clocked elements of Selvidge. It is certainly not clear that such a substitution would result in an operative device. The Examiner suggests that the virtual element and virtual clock of Selvidge is simply the detailed implementation of the programmable delay unit in Zeiner. However, this is incorrect. A programmable delay unit has entirely different operating characteristic than a clocked delay element. Moreover, making the proposed modification would change the fundamental operating principle of Zeiner.

Finally, admitting that Zeiner (and Selvidge) fails to teach or suggest the recited generating a test pattern, the Examiner relies on yet another reference, Dargelas for this further missing teaching. Specifically, the office action asserts that the abstract of Dargelas discloses generating a test pattern to test the circuit in accordance with the virtual clock signal for the virtual delay element. Applicants have thoroughly studied the abstract of Dargelas and can find no mention of virtual delay elements or virtual clocks. In any event, the Examiner has not provided an explanation of why one of ordinary skill in the art would be motivated to modify the hardware emulation system described by Zeiner to become or incorporate an automatic test pattern generator.

The office action simply fails to address the claim as a whole and impermissibly uses the claim as a blueprint to pick and choose selected pieces of the prior art.

Because there is no motivation to modify the teachings of Zeiner with the teachings of Selvidge, and with the further teachings of Dargelas, claims 22, 28, and 34 are patentable over the cited combination of references. Their respective dependent claims are likewise patentable.

With respect to claims 25, 31, and 37, the portion of Selvidge relied upon by the Examiner, namely col. 18, lines 65-67, describes a logical characteristic of the circuit, not a physical characteristic. Accordingly, the office action fails to establish a prima facie case and the claims are separately patentable for at least that reason.

With respect to claims 26, 32, and 38, the delay period described in col. 19, lines 1-14 of Selvidge does not appear to correspond to any physical characteristic of the circuit, but rather only to a logical propagation delay for logical states to settle. In any event, the VClk described in Selvidge is not specified in accordance with the alleged delay characteristic. Accordingly, the office action fails to establish a prima facie case and the claims are separately patentable for at least that reason.

With respect to claims 27, 33, and 39, the nested loops described in col. 19, lines 1-14 of Selvidge relate only to the logical structure and not the physical structure. The cited portion is devoid of any description related to lengths of conductive paths. Accordingly, the office action fails to establish a prima facie case and the claims are separately patentable for at least that reason.

In view of the foregoing, favorable reconsideration is respectfully requested. Early notification of the same is earnestly solicited. If there are any questions regarding the present application, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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